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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

7590 07/03/2002

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EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Advisory Action	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 6/05/02 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Attachment- A*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Samuel Broda

SAMUEL BRODA, ESQ.
PATENT EXAMINER

ATTACHMENT – A: ADVISORY ACTION

1. The examiner has reviewed the request for reconsideration under 37CFR §1.116 and request for withdrawal of premature finality. The final rejection is not premature. The applicant has made substantial amendments to the claims resulting in modifications of limitations and a change in the scope of the claimed invention, which necessitated citation of new reference. So the action was made final.

2. As per the argument that Hasegawa does not teach storing logical operation information in the library and in particular does not teach storing "logic operation information representing correspondence between a logical value of each input terminal and the logical value of each output terminal", as required by claims 1-4, the examiner respectfully disagrees with the applicant as explained below.

Blinne teaches determining the delay times of cells and integrated circuits using cell libraries. Hasegawa shows how the delay times at the input pins of an OR gate affects the delay time of the output pin of the OR gate as shown in Figs. 2, 3 and 5. The logic operation information representing correspondence between a logical value of each input terminal and the logical value of each output terminal is used in determining the delay time from input terminal to the output terminal, as per Col 2, Lines 31-42. So the circuit having shortest delay time affects the delay for the rising signal, while the circuit having longest delay affects the delay for the falling signal. The logic operation information is used in identifying an arc (circuit) as valid or invalid. If an AND gate was involved, then the logic operation information would again be used to determine the

delay time at the output pin and to identify the arc (circuit) as valid or not valid for the rise and fall signals. This is what is explained in Col 3, Lines 4-27, where the arcs are specified as invalid or valid. So Hasegawa uses the logic operation information to determine if an arc affects the delay time of the output signal or not. This also means that the logic operation information is stored in the computer as a file, or in a database or in the library.

In the application, Figure 6 shows the worst delay for the rising signals at the input pins of the AND gate. The worst delay is dependent on the longest delay at the input pins. So the input pin with the longest delay is valid and all other input pins and the circuits connected to them are invalid. Figure 7 shows the worst delay for the falling signals at the input pins of an AND gate. The worst delay is dependent on the shortest delay at the input pins for the falling signals. So the input pin with the shortest delay is valid and all other input pins and the circuits connected to them are invalid. The same logic operation information used in Hasegawa to determine the arcs as valid or invalid is used in application to compute the delay. So the method is same and the results are the same.

As argued in paper #8 (and summarized), it would have been obvious to one of ordinary skill in the art to combine the method of Hasegawa to compute the delays at the output pin taking into account the delays at the input pins and the logic operation information with the method of Blinne to compute delays for individual cells, as that would result in accurate determination of the delays in the circuits.

3. In view of the above explanation, the request for reconsideration has been considered but is not persuasive and does not place the application in condition for allowance.

K. Thangavelu
Art Unit 2123
June 21, 2002

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